IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application Serial No. 10/607,869
Filing Date ..... June 27, 2003
Inventor ..... Zhongze Wang
Assignee ..... Micron Technology, Inc.
Group Art Unit 2812
Examiner ..... Jennifer M. Kennedy
Attorney Docket No. MI22-2343
Title: Method of Forming Silicon-on-Insulator Comprising Integrated Circuitry

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References -- See Attached Form PTO-1449

The attached form PTO-1449 is submitted in compliance with 37 CFR §1.56. Copies of the cited art are included. No admission is made regarding whether all the submitted references are prior art.

Respectfully submitted,

Dated: June 10, 2005

By: Jennifer J. Taylor
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Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. MI22-2343	SERIAL NO. 10/607,869
	LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)	APPLICANT: Zhongze Wang	
		FILING DATE June 27, 2003	GROUP 2812

U.S. PATENT DOCUMENTS

*Examiner's Initials		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	6,071,783	6/2000	Liang et al.			
	AB	6,091,076	7/2000	Deleonibus			
	AC	6,245,636	7/2001	Maszara			
	AD	6,346,729	2/2002	Liang et al.			
	AE	6,358,791	3/2002	Hsu et al.			
	AF	6,403,485	6/2002	Quek et al.			
	AG	6,649,959	11/2003	Hsu et al.			
	AH	2002/0048844	4/2002	Sakaguchi			
	AI	2002/0034844	3/2002	Hsu et al.			
	AJ	10/924,776		Ford			08/25/2004
	AK						
	AL						

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

	AM		Bashir et al., *Characterization of sidewall defects in selective epitaxial growth of silicon*, 13 J. VAC. SCI. TECHNOL. B, No. 3, pp. 923-927 (May/June 1995).
	AN		Bashir et al., *Reduction of sidewall defect induced leakage currents by the use of nitrided field oxides in silicon selective epitaxial growth ...*, 18 J. Vac. Sci. Technol. B, No. 2, pp. 695-699 (March/April 2000).
	AO		Hammad et al., *The Pseudo-Two-Dimensional Approach to Model the Drain Section in SOI MOSFETs*, 48 IEEE TRANSACTIONS ON ELECTRON DEVICES, No. 2, pp. 386-387 (February 2001).
	AP		Sivagnaname et al., *Stand-by Current in PD-SOI Pseudo-nMOS Circuits*, IEEE, pp. 95-96 (June 2003)
	AQ		Wang et al., *Achieving Low Junction Capacitance on Bulk SI MOSFET Using SDOI Process*, Micron Technology, Inc., 12 pages (pre-2004).

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.